REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change I_{DDQ} in table IA. Add a footnote to table IA for V_{OL} and V_{OH}. Change limits in table IIB. - jak	07-07-19	Thomas M. Hess
B	Add die for device types 01 and 02 with die appendix A. Update radiation features in section 1.5 and add footnote 3/ for the device type 02. Delete class M requirements. - MAA	13-01-08	Thomas M. Hess

REV																				
SHEET																				
REV	B	B	B	B	B	B	B													
SHEET	15	16	17	18	19	20	21													

REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
Joseph A. Kerby

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Charles F. Saffle

APPROVED BY
Thomas M. Hess

DRAWING APPROVAL DATE
07-03-28

REVISION LEVEL
B

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

MICROCIRCUIT, DIGITAL, RADIATION HARDENED, LOW VOLTAGE CMOS, MINIMUM SKEW ONE-TO-EIGHT CLOCK DRIVER, LVTTL COMPATIBLE INPUTS AND OUTPUTS, MONOLITHIC SILICON

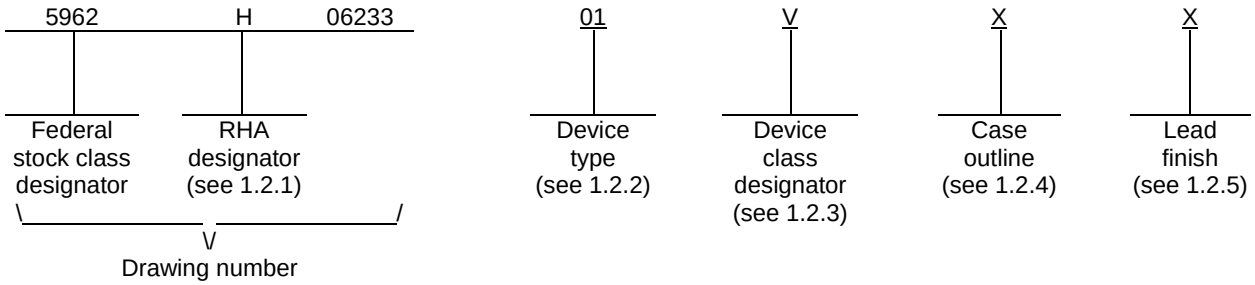
SIZE	CAGE CODE	
	67268	**5962-06233**

SHEET 1 OF 21

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ALVC2525	Minimum skew, one-to-eight clock driver, LVTTL compatible inputs and outputs
02	54ALVC2525	Minimum skew, one-to-eight clock driver, LVTTL compatible inputs and outputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	14	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

.

1.3 Absolute maximum ratings. 1/

Core power supply voltage range (V_{DD}) ..... -0.3 V dc to +4.0 V dc
Any clock input voltage range (V_{IN}) ..... -0.3 V dc to V_{DD} + 0.3 V dc
Any clock output voltage range (V_{OUT}) ..... -0.3 V dc to V_{DD} + 0.3 V dc
DC input current (I_I) ..... ±10 mA
Maximum power dissipation (P_D) ..... 1000 mW
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Maximum junction temperature (T_J) ..... +150°C 2/
Lead temperature (soldering, 10 seconds) ..... 260°C
Thermal resistance, junction-to-case (θ_{JC}) ..... 20 °C/W

1.4 Recommended operating conditions.

Core operating voltage range (V_{DD}) ..... +2.0 V dc to +3.6 V dc
Any clock input voltage range (V_{IN}) ..... +0.0 V dc to V_{DD}
Any clock output voltage range (V_{OUT}) ..... +0.0 V dc to V_{DD}
Case operating temperature range (T_C) ..... -55°C to +125°C

1.5 Radiation features.

Maximum total dose available (Dose rate = 50 – 300 rad(Si)/s):
Device type 01 ..... 1 Mrad(Si)
Device type 02 (effective dose rate = 1 rad (Si)/s) ..... 100 Krad(Si) 3/
Single event phenomenon (SEP):
No SEL occurs at effective LET (see 4.4.4.5) ..... ≤ 111 MeV/(cm^2/mg) 4/ 5/
No SEU occurs at on set LET (see 4.4.4.5) ..... ≤ 66 MeV/(cm^2/mg) 4/ 6/
(Saturated cross section=5.5 x 10^{-7} cm^2/device)
No SEU occurs at on set LET (see 4.4.4.5) ..... ≤ 52 MeV/(cm^2/mg) 4/ 7/
(Saturated cross section=8.7 x 10^{-7} cm^2/device)
Neutron irradiation ..... 1 X 10^{14} neutron/cm^2 4/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. This is a stress rating only, and functional operation for the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.

2/ Maximum junction temperature may be increased to +175°C during burn-in and steady state life tests.

3/ Device type 02 is irradiated at dose rate = 50 - 300 rad (Si)/s in accordance with MIL-STD-883, method 1019, condition A, and is guaranteed to a maximum total dose specified. The effective dose rate after extended room temperature anneal = 1 rad (Si)/s per MIL-STD-883, method 1019, condition A, section 3.11.2. The total dose specification for these devices only applies to the specified effective dose rate, or lower, environment.

4/ Limits are guaranteed by design or process but not production tested unless specified by the customer through the purchase order or contract.

5/ Worse case temperature and voltage of T_C = +125°C, V_{DD} = 3.6 V.

6/ T_C = 25°C, V_{DD} = 3.0 V, 200 MHz.

7/ T_C = 25°C, V_{DD} = 2.0 V, 200 MHz.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of this document are available online at http://www.astm.org/ or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA 19428-2959.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD20 Standard for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High-Speed CMOS devices.

JESD78 IC Latch-Up Test.

(Copies of these documents are available online at http://www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $+2.0\ V \le V_{DD} \le +3.6\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level input voltage	V_{IH}	V_{DD} = 2.0 V	1, 2, 3	All	1.25		V
		V_{DD} = 2.75 V		All	1.5		
		V_{DD} = 3.0 V		All	1.75		
		V_{DD} = 3.6 V		All	2.0		
Low level input voltage	V_{IL}	V_{DD} = 2.0 V	1, 2, 3	All		0.7	
		V_{DD} = 2.75 V		All		0.8	
		V_{DD} = 3.0 V		All		0.8	
		V_{DD} = 3.6 V		All		0.8	
Low Level output voltage	V_{OL}	I_{OL} = +12 mA, V_{DD} = 2.0 V	1, 2, 3	01		0.45	V
		I_{OL} = +12 mA, V_{DD} = 2.75 V	1, 2, 3	01		0.4	
		I_{OL} = +12 mA, V_{DD} = 3.0 V	1, 2, 3	01		0.4	
		I_{OL} = +12 mA, V_{DD} = 3.6 V	1, 2, 3	01		0.4	
	V_{OL} 2/	I_{OL} = +12 mA, V_{DD} = 2.0 V	1, 2, 3	02		0.45	V
		I_{OL} = +12 mA, V_{DD} = 2.75 V	1, 2, 3	02		0.4	
		I_{OL} = +12 mA, V_{DD} = 3.0 V	1, 2, 3	02		0.4	
		I_{OL} = +12 mA, V_{DD} = 3.6 V	1, 2, 3	02		0.4	
High level output voltage	V_{OH}	I_{OH} = -12 mA, V_{DD} = 2.0 V	1, 2, 3	01	1.5		V
		I_{OH} = -12 mA, V_{DD} = 2.75 V	1, 2, 3	01	2.2		
		I_{OH} = -12 mA, V_{DD} = 3.0 V	1, 2, 3	01	2.4		
		I_{OH} = -12 mA, V_{DD} = 3.6 V	1, 2, 3	01	3.0		
	V_{OH} 2/	I_{OH} = -12 mA, V_{DD} = 2.0 V	1, 2, 3	02	1.5		V
		I_{OH} = -12 mA, V_{DD} = 2.75 V	1, 2, 3	02	2.2		
		I_{OH} = -12 mA, V_{DD} = 3.0 V	1, 2, 3	02	2.4		
		I_{OH} = -12 mA, V_{DD} = 3.6 V	1, 2, 3	02	3.0		
Short circuit output current	I_{OS}	V_{OUT} = V_{DD} and V_{SS}, V_{DD} = 2.0 V	1, 2, 3	All	-200	200	mA
	3/	V_{OUT} = V_{DD} and V_{SS}, V_{DD} = 3.6 V	1, 2, 3	All	-300	300	
Input leakage current	I_{IL}	V_{IN} = V_{DD} or V_{SS}, V_{DD} = 3.6 V	1, 2, 3	All	-1	+1	µA
Quiescent supply current	I_{DDQ}	V_{DD} = 2.0 V	1, 2, 3	All		1.0	mA
		V_{DD} = 3.6 V	1, 2, 3	All		1.0	
Total power dissipation	P_D	V_{DD} = 2.0 V, C_L = 20 pF	1, 2, 3	All		1.2	mW/ MHZ
	4/	V_{DD} = 2.75 V, C_L = 20 pF		All		2.7	
		V_{DD} = 3.0 V, C_L = 20 pF		All		3.5	
		V_{DD} = 3.6 V, C_L = 20 pF		All		5.2	
Input capacitance	C_{IN}	f = 1 MHz V_{DD} = 0 V	4	All		15	pF
Output capacitance	C_{OUT}	f = 1 MHz V_{DD} = 0 V	4	All		15	pF
Functional tests		See 4.4.1b	7, 8	All			

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $+2.0\ V \le V_{DD} \le +3.6\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Propagation delay time, high-to-low, CLK to On	t_{PHL} 5/	Measured as transition time between $V_{IN} = V_{DD}/2$ to $V_{OUT} = V_{DD}/2$	V_{DD} = 2.0 V	1, 2, 3	All	3.5	7.5	ns
			V_{DD} = 2.75 V		All	3.0	5.5	
			V_{DD} = 3.0 V		All	2.75	5.25	
			V_{DD} = 3.6 V		All	2.25	4.75	
Propagation delay time, low-to-high, CLK to On	t_{PLH} 5/	Measured as transition time between $V_{IN} = V_{DD}/2$ to $V_{OUT} = V_{DD}/2$	V_{DD} = 2.0 V	9, 10, 11	All	3.25	7.25	ns
			V_{DD} = 2.75 V			2.75	5.25	
			V_{DD} = 3.0 V			2.5	5.0	
			V_{DD} = 3.6 V			2.0	4.5	
Maximum skew, common edge, output-to-output, high-to-low transition	t_{OSHL} 5/, 6/	V_{DD} = 2.0 V		9, 10, 11	All		0.15	ns
		V_{DD} = 3.6 V					0.25	
Maximum skew, common edge, output-to-output, low-to-high transition	t_{OSLH} 5/, 6/	V_{DD} = 2.0 V		9, 10, 11	All		0.15	ns
		V_{DD} = 3.6 V					0.25	
Input rise or fall time	t_r, t_f 3/	V_{IH} minimum, V_{IL} = (maximum)		9, 10, 11	All		20	ns/V
Output rise or fall time	t_{ORISE}, t_{OFALL} 3/	Measured as transition time between 20%V_{DD} and 80%V_{DD}.	V_{DD} = 2.0 V	9, 10, 11	All		2.4	ns
			V_{DD} = 3.6 V				2.0	
Part to part skew	t_{PART} 5/, 6/	Skew between the outputs of any two devices under identical settings and conditions.	V_{DD} = 2.0 V	9, 10, 11	All		0.10	ns
			V_{DD} = 3.6 V				0.15	
Propagation delay balance: difference between same output, low-to-high and high-to-low transitions	t_{PBAL} 5/	Measured as transition time between, $V_{IN} = V_{DD}/2$ to $V_{OUT} = V_{DD}/2$	V_{DD} = 2.0 V	9, 10, 11	All		0.43	ns
			V_{DD} = 2.75 V				0.30	
			V_{DD} = 3.0 V				0.26	
			V_{DD} = 3.6 V				0.21	

1/ RHA parts for device type 01 supplied to this drawing have been characterized through all levels M, D, P, L, R, F, G, and H of irradiation. However, this device is only tested at the 'H' level.
RHA parts for device type 02 supplied to this drawing have been characterized through all levels M, D, P, L, and R of irradiation. However, this device is only tested at the 'R' level. Device type 02 is irradiated at dose rate = 50 - 300 rads (Si)/s in accordance with MIL-STD-883, method 1019, condition A, and is guaranteed to a maximum total dose specified. The effective dose rate after extended room temperature anneal = 1 rad (Si)/s per MIL-STD-883, method 1019, condition A, section 3.11.2. The total dose specification for these devices only applies to the specified effective dose rate, or lower, environment.
Pre and Post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, $T_A = +25°C$.
2/ For RHA levels F, G, and H, device type 02 disables the outputs and will not pass V_{OL} and V_{OH} test conditions.
3/ Supplied as a design limit. Neither guaranteed nor tested.
4/ When measuring the dynamic supply current, all outputs are loaded in accordance with the equivalent test lead defined in figure 4.
5/ Test load C_L = 40 pF, terminated to $V_{DD}/2$. All outputs are equally loaded. Refer to figure 4 for clock output loading.
6/ Guaranteed by characterization, but not tested.

TABLE IB. SEP test limits. 1/ 2/

Device type	Single event upset (SEU) 3/		Single event latchup (SEL) 4/
	Effective LET [MeV/(mg/cm^2)]	Maximum device cross section (cm^2)	No latch-up Bias V_{DD} = 3.6 V Effective LET [Mev/(mg/cm^2)]`
All	66 5/ 52 6/	5.5×10^{-7} 5/ 8.7×10^{-7} 6/	111

1/ Devices that contain cross coupled resistance must be tested at the maximum rated T_C. For SEP test conditions, see 4.4.4.5 herein.

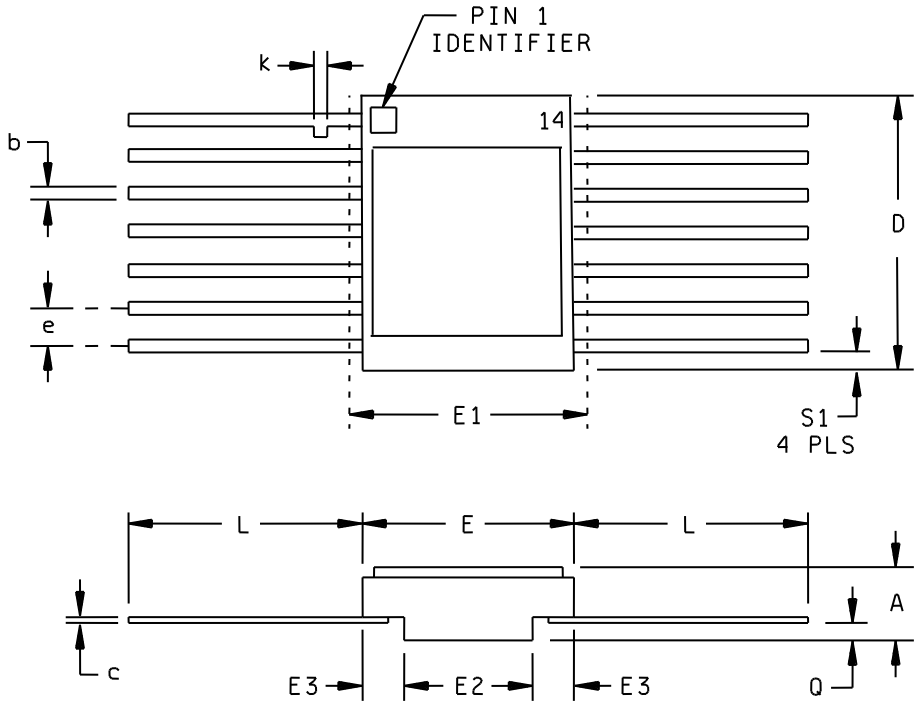
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line. Test plan must be approved by TRB and qualifying activity.

3/ T_C = +25°C ±10°C

4/ T_C = +125°C ±10°C

5/ V_{DD} = 3.0 V, 200 MHz

6/ V_{DD} = 2.0 V, 200 MHz



Dimensions				
Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	0.079	0.101	2.01	2.57
b	0.015	0.019	0.38	0.48
c	0.004	0.007	0.10	0.18
D	0.333	0.347	8.46	8.81
E	0.250	0.260	6.35	6.60
E1	- - -	0.290	- - -	7.37
E2	0.170	0.180	4.32	4.57
E3	0.030	- - -	0.76	- - -
e	0.050 BSC		1.27 BSC	
L	0.340	0.360	8.64	9.14
Q	0.026	- - -	0.66	- - -
S1	0.005	- - -	0.13	- - -

FIGURE 1. Case outline.

Device types	01, 02
Case outline	X
Terminal number	Terminal symbol
1	O0
2	O2
3	NC
4	GND
5	V_{DD}
6	O4
7	O6
8	O7
9	O5
10	GND
11	V_{DD}
12	CLK
13	O3
14	O1

NC = No connection

Terminal descriptions	
Terminal symbol	Description
CLK	Clock input
On (n = 0 to 7)	Outputs

FIGURE 2. Terminal connections.

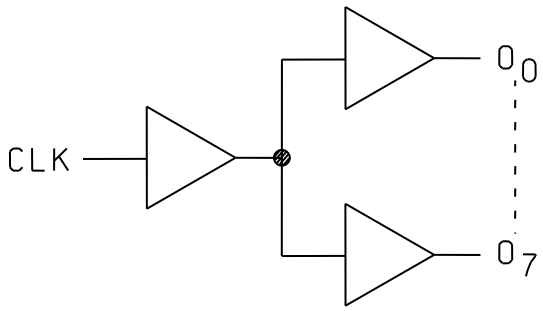
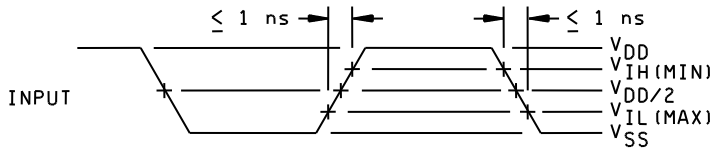
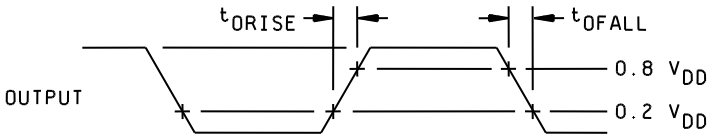


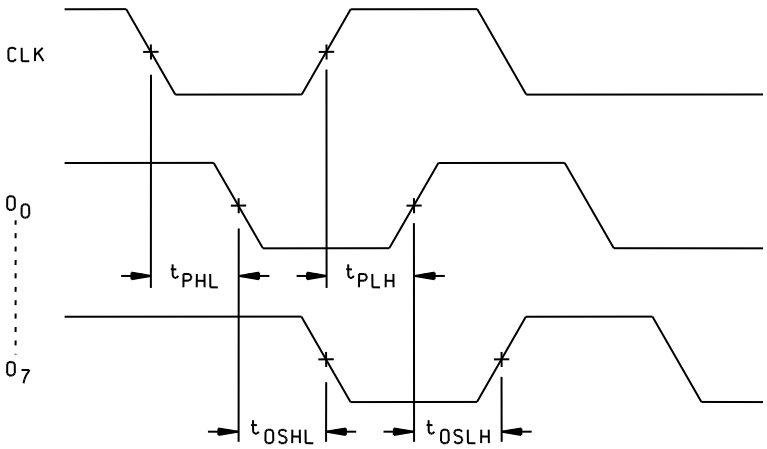
FIGURE 3. Block diagram.



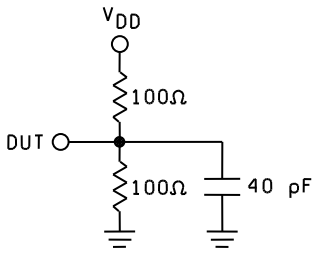
CLK INPUT TEST WAVEFORM



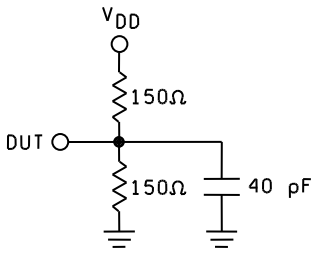
OUTPUT TEST WAVEFORM



AC TIMING DIAGRAM



TEST LOAD CIRCUIT FOR DYNAMIC POWER SUPPLY CURRENT, t_{PHL}, t_{PLH}, t_{PBAL}, AND t_{PART}



TEST LOAD CIRCUIT FOR CHARACTERIZATION OF OUTPUT SKEW PARAMETERS (t_{OSHL}, t_{OSLH})

FIGURE 4. Switching waveforms and test circuit.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/ 3/
Group A test requirements (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11 3/
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 2, 3, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.
3/ Delta limits, as specified in table IIB herein, shall be required when specified and the delta values shall be completed with reference to the zero hour electrical parameter.

TABLE IIB. Burn-in delta parameters (+25°C).

Parameter	Symbol	Condition	Limits
Supply current	I_{DDQ}	V_{DD} = 3.6 V, T_A = 25°C	± 980 μA

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured herein.

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein.

4.4.4.1.1 Accelarated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Neutron testing. When required by the customer, neutron testing shall be performed in accordance with test method 1017 of MIL-STD-883 and herein. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in table IIA herein at T_A = 25°C ±5°C after an exposure of 2 X 10^{12} neutrons/cm^2 (minimum).

4.4.4.3 Dose rate induced latchup testing. When required by the customer, dose rate induced latchup testing shall be performed in accoradance with test method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.4 Dose rate upset testing. When required by the customer, dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD883 and herein.

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may affect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

4.4.4.5 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test 4 devices with 0 failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C for SEU testing and + 125°C for SEL testing ±10°C.

f. Bias conditions shall be V_{DD} = 2.0 V dc and 3.0 V dc, V_{DD} =3.6 V dc for latchup measurements.

g. For SEP test limits, see table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA Test conditions (SEP).

b. Number of upsets (SEU).

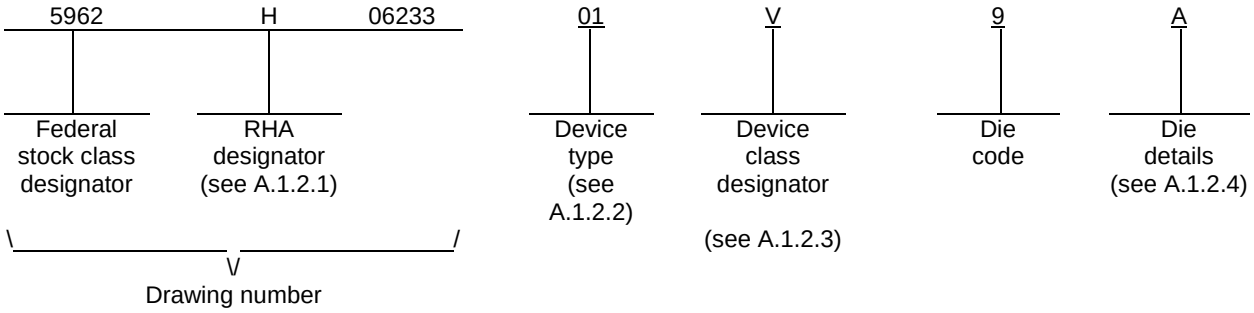
c. Occurrence of latchup (SEL).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-06233

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardiness Assurance (RHA) levels is reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ALVC2525	Minimum skew, one-to-eight clock driver, LVTTL compatible inputs and outputs
02	54ALVC2525	Minimum skew, one-to-eight clock driver, LVTTL compatible inputs and outputs

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535.

A.1.2.4 Die Details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01	A-1
02	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01	A-1
02	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01	A-1
02	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01	A-1
02	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-06233

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specifications, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits Manufacturing, General Specification For.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and figure A-1.

A.3.2.5 Truth table. The truth table shall be as defined in paragraph 3.2.3 herein.

A.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.6 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not effect the form, fit or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a) Wafer lot acceptance for Class V product using the criteria defined in MIL-STD-883 method 5007.

b) 100% wafer probe (see paragraph A.3.4 herein).

c) 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883 method 2010 or the alternate procedures allowed in MIL-STD-883 test method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table II herein. Group E tests and conditions are as specified in paragraphs 4.4.4 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime-VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0547.

A.6.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

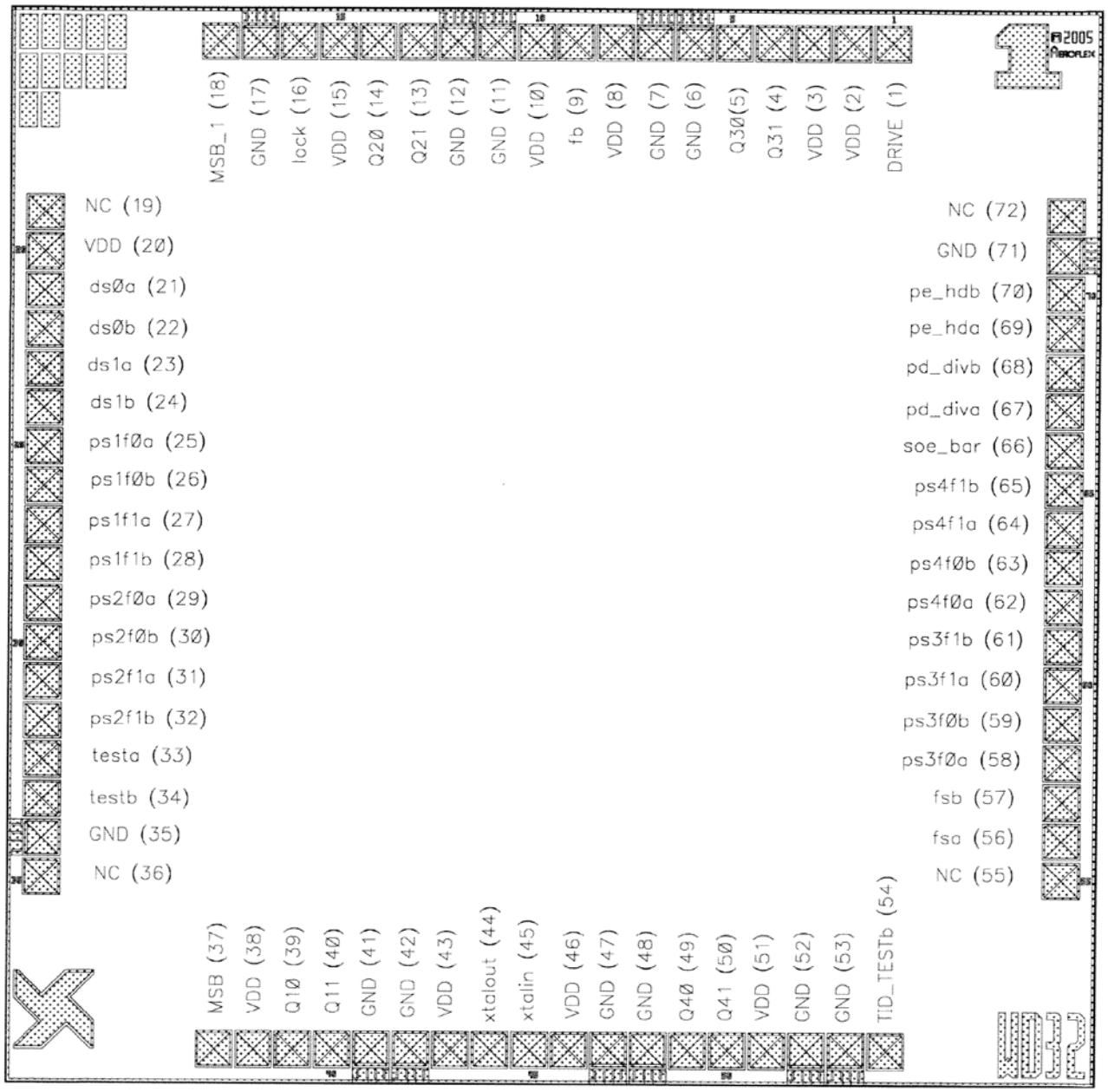


FIGURE A-1. Die bonding pad locations and electrical functions.

Die physical dimensions.

Die size:	101.57mils x 101.57 mils
Die thickness:	17.5 $\pm$0.5 mils

Interface materials.

Top metallization:	Si Al Cu
Thickness:	6.2 k Å - 11 k Å
Backside metallization:	None
Glassivation.	
Type:	SiO_2/Si_3N_4
Thickness:	9.0k Å - 11.0 k Å
Substrate:	Epitaxial Layer on Single Crystal Silicon

Assembly related information.

Substrate potential:	Tied to V_{SS} /Ground
Special assembly instructions:	Bond all V_{SS}/Ground and V_{DD} die pads.

FIGURE A-1. Die bonding pad locations and electrical functions.- Continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 13-01-08

Approved sources of supply for SMD 5962-06233 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962H0623301QXA	65342	UT54ALVC2525
5962H0623301QXC	65342	UT54ALVC2525
5962H0623301VXA	65342	UT54ALVC2525
5962H0623301VXC	65342	UT54ALVC2525
5962R0623302QXA	65342	UT54ALVC2525
5962R0623302QXC	65342	UT54ALVC2525
5962R0623302VXA	65342	UT54ALVC2525
5962R0623302VXC	65342	UT54ALVC2525
5962H0623301Q9A	65342	UT54ALVC2525H-QDIE
5962R0623302Q9A	65342	UT54ALVC2525R-QDIE
5962H0623301V9A	65342	UT54ALVC2525H-VDIE
5962R0623302V9A	65342	UT54ALVC2525R-VDIE

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65342	Aeroflex Colorado Springs, Inc. 4350 Centennial Boulevard Colorado Springs, CO 80907-3486